Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1 - 84 (CANCELLED)

85. (NEW) An apparatus for inserting a DFD (design-for-debug) circuitry in an integrated circuit to debug or diagnose selected fault types in scan cores, the integrated circuit containing two or more said scan cores each having a scan clock; said apparatus comprising:

(a) a DFD selector for indicating which said scan cores and said selected fault types will be debugged or diagnosed simultaneously;

(b) a scan connector for connecting multiple scan chains in said scan cores to a boundary-scan chain in said integrated circuit;

(c) a scan clock generator for generating an ordered sequence of capture clocks for connection to said scan clocks in said scan cores; and

(d) a multiplexer for connecting said DFD selector and said scan connector to a TAP (test access port) controller in said integrated circuit.

86. (NEW) The apparatus of claim 85, further comprising a scan debug mode; wherein said scan debug mode is set to logic value 1 when said scan cores are to be diagnosed, and set to logic value 0 when said scan cores are not to be diagnosed;

87. (NEW) The apparatus of claim 86, wherein said scan debug mode is generated by a central DFD controller; wherein said central DFD controller interfaces with said TAP controller and said DFD circuitry; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard which includes a test access port (TAP) comprising TDI (test data in), TDO (test data out), TCK (test clock), TMS (test mode select), and selectively TRSTB (test reset).

88. (NEW) The apparatus of claim 85, wherein said faults chosen by said selected fault types further comprise stuck-type faults and non-stuck-type delay faults; wherein said stuck-type faults include stuck-at faults, bridging faults, and IDDQ (IDD quiescent current) faults; and wherein said non-stuck-type delay faults include transition (gate-delay) faults, path-delay faults, memory read/write faults, and multiple-cycle delay faults.

89. (NEW) The apparatus of claim 87, wherein said DFD selector further comprises using a shift register of 2 or more bits in each said scan core to indicate whether said scan core will be

diagnosed and what said selected fault type shall be targeted; wherein said shift register is controlled by said TCK and its scan data input and scan data output are connected to said TDI and said TDO via said multiplexer, respectively.

90. (NEW) The apparatus of claim 87, wherein said scan connector further comprises using a plurality of multiplexers to stitch said multiple scan chains together as one serial scan chain and connect its scan data input and scan data output to said TDI and said TDO, respectively; wherein said multiplexers are controlled by said scan debug mode.

91. (NEW) The apparatus of claim 87, wherein said scan connector further comprises using a plurality of multiplexers to stitch said multiple scan chains together as one serial scan chain and insert said serial scan chain before or after said boundary-scan chain; wherein said multiplexers are controlled by said scan debug mode.

92. (NEW) The apparatus of claim 87, wherein said scan connector further comprises using a plurality of multiplexers to stitch only those scan cells within all said multiple scan chains which share the same said scan clock together as one single scan chain, called grouped scan chain; wherein said grouped scan chain connects its scan data input and scan data output to said TDI and

said TDO, respectively; and wherein said multiplexers are controlled by said scan debug mode.

93. (NEW) The apparatus of claim 85, wherein said scan connector further comprises selectively inserting an inverter and a lock-up element between any two said multiple scan chains when stitched together to form a serial scan chain or a grouped scan chain; wherein said lock-up element is a selected D latch or D flip-flop.

94. (NEW) The apparatus of claim 87, wherein said scan clock generator for generating an ordered sequence of capture clocks further comprises a clock phase generator and a scan clock controller.

95. (NEW) The apparatus of claim 94, wherein said clock phase generator is controlled by said TCK and generates a plurality of non-overlapping TCK clocks; and wherein said scan clock controller is controlled by said selected fault type and connects said capture clocks, comprising said TCK, said non-overlapping TCK clocks, and non-overlapping system clocks, to said scan clocks in said scan cores; wherein said non-overlapping system clocks are generated by the system clocks external to said integrated circuit or on an ATE (automatic test equipment).

96. (NEW) The apparatus of claim 95, wherein said non-overlapping TCK clocks are used to debug or diagnose said stuck-type faults, including said stuck-at faults, said bridging faults, and said IDDQ faults, in said scan cores in said integrated circuit.

97. (NEW) The apparatus of claim 95, wherein said non-overlapping system clocks are used to debug or diagnose said non-stuck-type delay faults, including said transition (gate-delay) faults, said path-delay faults, said memory read/write faults, and said multiple-cycle delay faults, in said scan cores in said integrated circuit.

98. (NEW) The apparatus of claim 95, wherein said scan clock controller further comprises a generator for generating a global scan enable (GSE) signal to control the shift and capture operations of said multiple scan chains in said scan cores; wherein said generator for generating a global scan enable (GSE) signal is further generated by said TAP controller, including Shift_DR, Capture_DR, and Update_DR, according to said selected Boundary-scan Standard.

99. (NEW) The apparatus of claim 85, wherein said DFD circuitry is further selected for debugging or diagnosing memory scan cores.

100. (NEW) A method for debugging or diagnosing selected fault types in scan cores using an embedded DFD (design-for-debug) circuitry in an integrated circuit, the integrated circuit containing two or more said scan cores each having a scan clock; said method comprising the steps of:

(a) issuing a DBG_SCAN command for generating a scan debug mode to control said DFD circuitry in said scan cores;

(b) issuing a SELECT command for shifting in selected scan cores and said selected fault types to be debugged or diagnosed to the DFD selector of said DFD circuitry in said scan cores;

(c) issuing a first SHIFT command or a first plurality of SHIFT_CHAIN commands for shifting in a predetermined scan pattern to all scan cells within selected scan chains in said scan cores for diagnosis;

(d) issuing one or more CAPTURE commands for capturing output responses into all said scan cells in said scan cores;

(e) issuing a second SHIFT command or a second plurality of SHIFT_CHAIN commands for shifting a new predetermined scan pattern into and output response out of all said scan cells within said selected scan chains in said scan cores for diagnosis;

(f) repeating steps of (d)-(e) until scan diagnosis is done; and

(g) issuing a STOP command for generating a stop control signal to stop the scan operation.

101. (NEW) The method of claim 100, further comprising providing a central DFD controller for accepting said commands and generating said scan debug mode and said stop control signal to control said DFD circuitry; wherein said DFD controller interfaces with said DFD circuitry and a TAP (test access port) controller in said integrated circuit; and wherein said TAP controller is constructed according to a selected Boundary-scan Standard.

102. (NEW) The method of claim 100, wherein said faults chosen by said selected fault type in said selected scan core for debug or diagnosis further comprise selectively stuck-type faults or non-stuck-type delay faults; wherein said stuck-type faults include stuck-at faults, bridging faults, and IDDQ faults; and wherein said non-stuck-type delay faults include transition (gate-delay) faults, path-delay faults, memory read/write faults, and multiple-cycle delay faults.

103. (NEW) The method of claim 100, wherein said commands are further used to debug or diagnose memory scan cores.